EUROPEAN VLBI NETWORK

Institute of Applied Astronomy
of the Russian Academy of Sciences

Extending the Facilities of BRAS by External Digital Downconverter Bank

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1. Introduction

Broadband Acquisition Systems (BRAS) are used on fast slew radio telescopes RT-13 of "Quasar-KVO" complex [1-5]. The BRAS allows to register wideband signals of 512 MHz, that provides the necessary sensitivity for astrometrical observations. However, most existing VLBI radio telescopes still use data acquisition systems with narrowband channels (up to 16 MHz bandwidth). It greatly complicates the processing of joint observations of RT-13 with other VLBI radio telescopes.

To achieve a compatibility of RT-13 with radio telescopes, equipped with narrow-band data acquisition systems, BRAS will be supplement with an external digital downconverter bank (DDCB). The posters presents principles, features and implementation details of DDCB.

2. The purpose and structure of the system

Most of the VLBI observations are carried out in international networks using a frequency synthesis method in S and X frequency bands [6]. An arrangement range 6 narrowband channels in the S band is 270, which does not exceed the BRAS channel bandwidth. For a standard arrangement of 8 narrowband channels in X band (720 MHz) two channels of BRAS are required. Thus, DDCB must simultaneously receive the digital data from three channels of BRAS and convert it to 14 independent narrowband channels. The input data format for DDCB is VDIF (VLBI Data Interchange Format [7]). The data rate (2 or 8 Gbit/s) of wideband channels are depend on the amount of bits per sample (2 or 8 bit). For compatibility with existing data buffering and transmission system [8] output format is VDIF. The output data stream contains selected portions of the spectra width of 8 or 16 MHz (up to 14 parts) of any part of the three input wideband signal and does not exceed 4,096 Mbit / s (including the fact that the bit data output of 8 bits, and the number of channels supplemented by two "zero" tracks and total number of channels is 16 (in accordance with VDIF requirements).

DDCB (Fig. 1) includes three optical transceiver that provide the physical layer for transmitting and receiving the data flows through the 10 Gbit / s Ethernet fiber-optic lines (FOL), the module for digital signal conversion by the field programmable logic gate array (FPGA), Ethernet interface controller and the oscillators of reference signals.

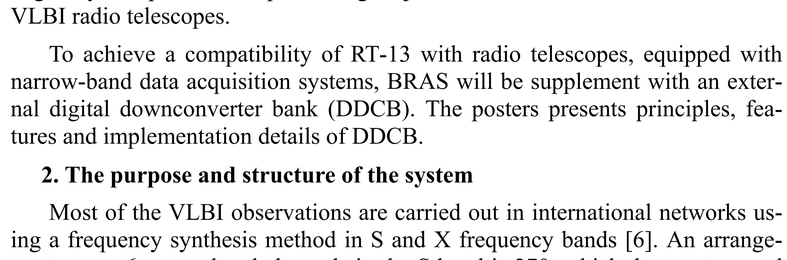

Fig. 1. Block diagram of the bank external digital downconverters for the BRAS.

Internet packets containing VDIF data, introduced in FPGA through GTX receiving ports using 10-gigabit SFP + transceivers. FPGA performs the next operations: buffering data, transformation specified spectrum areas to video frequency, formation an output data, containing 14 narrowband channels in VDIF format. Output data from FPGA GTX port through the optical transceiver SFP + are transmitted to the data buffer device by 10GE Interface.

DDCB is controlled by a radio telescope central computer via 10/100/1000 Ethernet interfaces that implemented on a chip Marvell 88E1111 conjugated with FPGA. Microblaze processor for control is implemented in the FPGA configuration.

3. The digital signal conversion unit

Digital converter unit is implemented on FPGA XC7325T-2FFFG900 and contains three independent data buffers, the three prefilters, 14-channel switch and 14 digital frequency converters. The processing of digital flows in each downconverter is divided into several stages: separation of the upper and lower sideband signal after prefiltration stage, moving a predetermined portion of the spectrum to lower frequencies, video bandwidth forming and subsequent formation of two-bit data flow. In addition, the FPGA configuration contain timer, VDIF frame data pack unit, Ethernet frame pack unit, data-capture module and Microblaze control processor (Fig. 2).

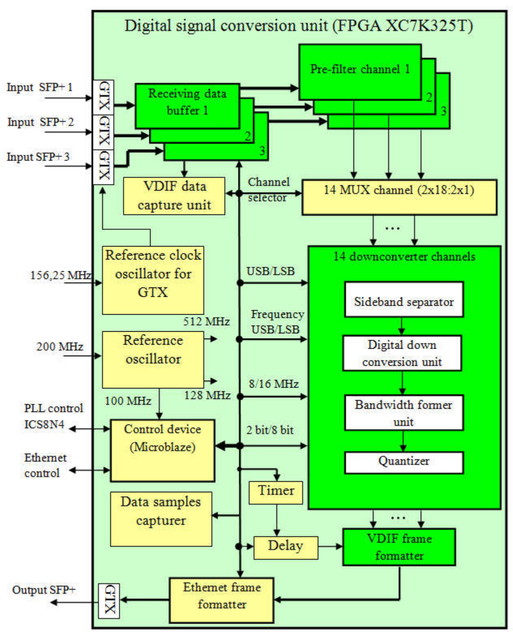

Fig. 2. Block diagram of digital conversion unit

Each data buffer unit parses packet headers and extracts the data sequences, then restores continuous digital data stream with rate of up to 8 Gb / s (eight eight-bit samples with a clock frequency of 128 MHz). Prefiltration is produced by polyphase filter with was constructed on the discrete Fourier transform (DFT) basis with pre-formed an amplitude frequency characteristic (AFC) by using a weighting function. The calculation of polyphase decomposition of signals is carried out according to the formula [9]:

$$y_k[n_k] = \sum_{i=0}^{M-1} h_k x[n_k] W_M^{-ki}$$

there M – the number of channels for polyphasic decomposition (the size of DFT), y_k – the samples of signal on the k-filters exit (k=0…M – 1), x – digital signal on the input of polyphasic filter; h – the weight function of analysis filter for pre-forming of filters frequency response, $W_M = e^{\frac{-j2\pi}{M}}$ – the complex Fourier transform's coefficient, n_k=integer(t/M)+k – the number of samples for channel k, t – the number of samples for filter input sequency, $j = \sqrt{1}$.

The choice coefficients of a weighting function substantially affects the channel impulse response and polyphase energy distribution between the main and side lobes of its spectral function. Therefore, to minimize the effects of spectral leakage in accordance with the recommendations in [10] the weighting function coefficients was calculated by the formula:

$$h[i] = \frac{1}{2} - \frac{1}{2}\cos\left(\frac{2\pi i}{pM}\right)\mathrm{sinc}\left(\frac{i - pM/2}{p}\right)$$

there p – order of the weighting function filter shaper in the channel of polyphase filter, i = 0...pM.

The order for shaping filters is chosen equal to 8. The initial bandwidth of 512 MHz is divided into M = 8 overlapping ranges of 128 MHz. The advantage of this signal prefiltering with the partition is the save FPGA resources and the relative ease of implementation. Disadvantages of this method include the fact that i 128 MHz (i = 0 ... M–1) frequency of signal is transformed to the zero frequency ("blind zone"), as well as necessary to deal with a quadrature signal. The transform of any signal portion in the band 0 – 512 MHz, including those frequencies around 128 i MHz ± Δf, where Δf – bandwidth video filter output (in this case, 8 or 16 MHz) is provided through a complementary additional quadrature converter to 32MHz (Fig. 3), which provide the possibility to processing of "blind spots".

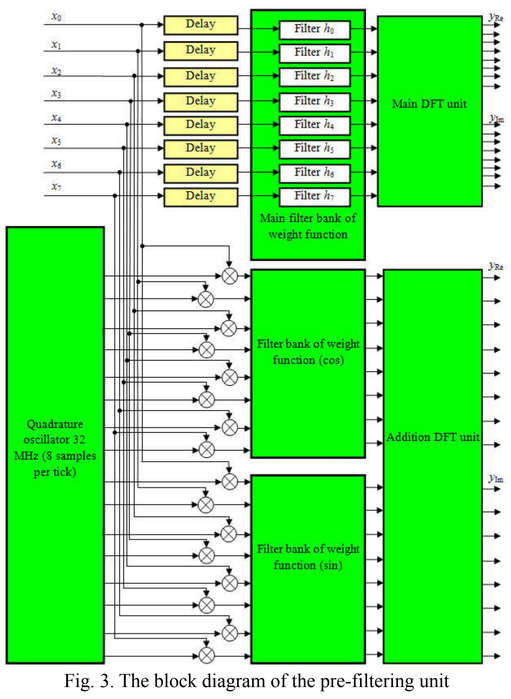

Fig. 3. The block diagram of the pre-filtering unit

The AFC of 5 major prefiltered zones (solid lines) and 3 shifted by 32 MHz zones (dashed line) are shown in Fig. 4.

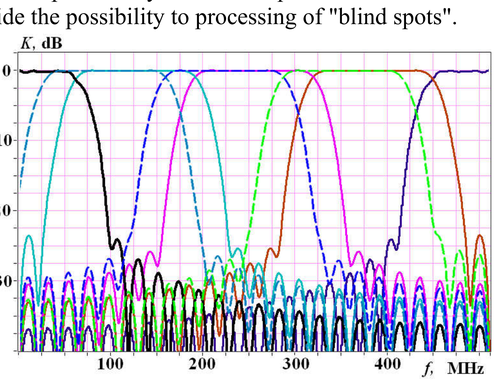

Fig. 4. The AFC of major pre-filtered zones (solid lines) and shifted by 32 MHz zones (dashed line)

Through switch quadrature signals are fed to the sidebands separator. Separation sideband is performed by phase method. To ensure to lower the operating frequency downconverter at least 1 MHz (in this frequency usually located the phase calibration signal), the broadband phase shift of one of the quadrature signals is required [11]. In accordance with the procedure signal has to pass through the sine and cosine filters. The frequency response of the filter is based on a prototype filter. The sine filter has phase shift 90° comparison to the cosine filter. In order to ensure the passage of the signal at a frequency of 1 MHz with a bandwidth of, for example, 32 MHz, requires the implementation of a narrow transition zone frequency response (0.3% of the Nyquist frequency). The hardware implementation of narrow transition zone with direct methods requires a large number of FPGA resources (the number of taps of the filter is inversely proportional to transition zone), such as hardware multipliers, and in this case, due to the rather large number of channels is not applicable. To effectively use the resources of the FPGA low-frequency spectrum of the signal is advantageous to process separate from the main part of the spectrum, simplifying the process and the last [12]. It is also used for minimize the number of multipliers the method of multiuse FPGA resources with decreasing frequency (decimation) of the input signal. In accordance with the method that described in [12], the signal band with the prefilter output is divided into three sub-band (Fig. 5).

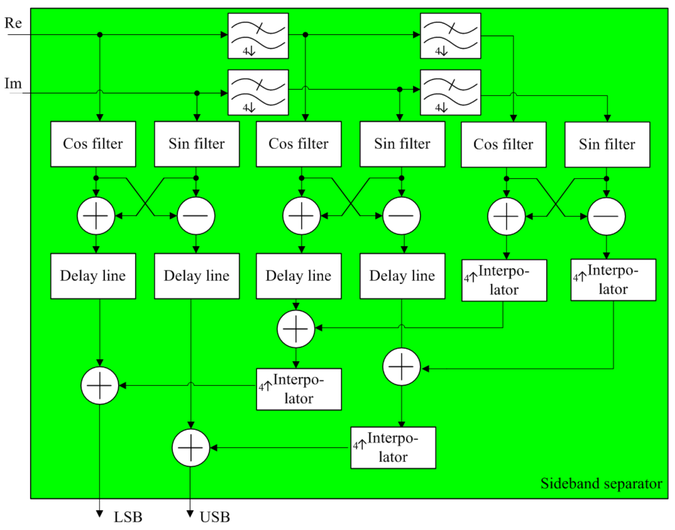

Fig. 5. The block diagram of sidebands separator .

To troubleshoot 'bundled' sine filter frequency response at higher frequencies close to the Nyquist frequency, in the structure included two spectrum inverters - one inlet and one outlet. The total bandwidth of the filter separator is chosen equal from 0.15 to 52 MHz, and if necessary, the spectrum processing section, starting from 52 MHz up to the Nyquist frequency with spectrum inversion mode by "switch on" inverters at the inlet and outlet. The frequency dependence of sideband suppression coefficient and the frequency response are shown in Fig. 6. As can be seen from the graph, the coefficient suppressing the side bands in most of the working strip of separator is no less than 35 dB.

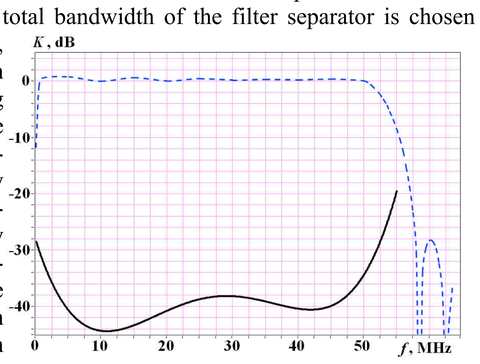

Fig. 6. AFC (dotted line) and coefficient of sideband suppression (solid line).

The next step of processing is performed by digital transformation of the signal. The frequency converter comprises (Fig. 7) quadrature mixer, quadrature frequency oscillator that operating in a range of 0 – 63.99 MHz, filter-decimator with a decimation factor of 2 times and sidebands separator, operating from 0.1 to 25 MHz. Sidebands separator is built on the principles described above, but additionally uses a partition of the entire frequency band signal into 3 sub-band. The output of the frequency converter is switchable filter 8/16 MHz. Step of quadrature tuning oscillator, that constructed on the basis of the sine and cosine tables, is 10 kHz.

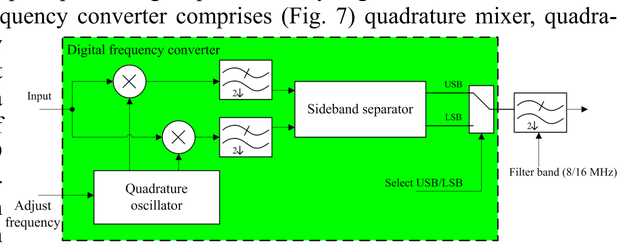

Fig. 7. The block diagram of frequency signal transformation unit

Two-bit quantizer with floating threshold is based on calculating the RMS value of signal σ_u on a predetermined time interval and comparators. The quantization of the amplitudes on the levels is performed in accordance with the following relationships: $u < -\sigma_u$, $-\sigma_u < u < 0$, $0 < u < \sigma_u$ и $u > \sigma_u$, there u – the instantaneous value of the voltage.

The output formatter of VDIF-frame integrates the data from downconverter outputs into total flow, which is then broken up into packets of a given size. The frame headers include service information obtained by decoding the input data from BRAS, and additional parameters DDCB. These observations together with service information packed in "raw" Ethernet-packets with the possible addition of UDP and IP headers, that transmitted through the interface to the transceiver 10GE receiver-transmitter and a next to the data buffering device on radio telescope.

4. The software

The controller was made on the basis of Microblaze-processor, which formed in FPGA, is the main element of DDCB management system. Upon request, obtained via Ethernet, the controller forms the response, which contains control information (e.g., synchronization check, presence of transceivers and others). The obtained data are used to control system operation.

The system is controlled by a radio telescope central computer through the 10/100/1000 Ethernet interface. To communicate with a computer through UDP FPGA use Ethernet-controller PHY 88E1111 and GMII interface. Text commands of UDP-packets from control computer are processed by Microblaze-processor which was formed in FPGA.

All control and monitoring functions are implemented in the control program which written in C ++ in a cross-platform environment for programming Qt 4.8. An example of the main tab of the graphical interface of the program on the computer screen is shown in Fig. 8.

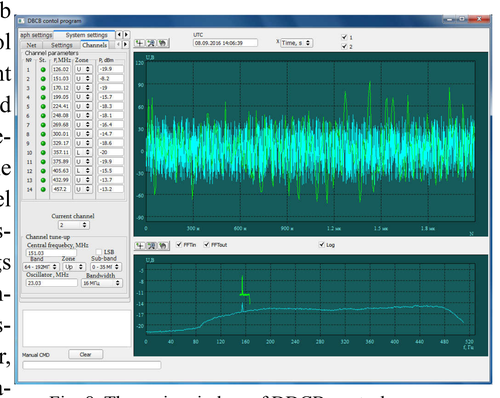

Fig. 8. The main window of DDCB control program

On the main tab ("Channels") of the control program displays the current settings of each narrowband channel and power measurement data, display the "correctness" of the channel signals quantization statistics, as well as the settings panel of the parameter channel. On the "Settings" is displayed current system timer, the presence of synchronization with the time scale and time of commencement and completion of the "record". From this tab, you can set the time or select the reference data channel with which synchronization is performed. Set configuration and data transfer modes via 10G Ethernet can use with the "Recording Settings" tab. Tab «Inputs 10G» allows you to customize the behavior of foster 10G transceivers, as well as the control data received by the capture of data from VDIF-frame. Signal data are displayed as a waveform and spectrum, and service information from headers VDIF frames displayed in a tabular format.

5. Conclusion

The main DDCB components were developed and debugged: data buffer, prefiltering, sidebands separator and digital down convertor, and output signal quantizer. The final adjustment of developed firmware is carrying out to optimize FPGA resource utilization. Laboratory tests of DDCB are currently performing and the first test in real observations has to be performed until the end of 2016.

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