Extending the Facilities of BRAS by External Digital Downconverter Bank

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Broadband Acquisition System (BRAS) is a digital backend used on new fast-slew rate radiotelescopes RT-13. The system implements eight wideband channels of 512 MHz that allows to achieve high sensitivity of the radio interferometer but complicates processing of joint observations with narrow-band types of backends. To simplify such observations IAA RAS is developing external digital downconverter bank. The results of the development is presented.

Keywords: VLBI DAS, BRAS, digital downconverter bank.

1 Introduction

Broadband Acquisition Systems (BRAS) are used on fast slew radio telescopes RT-13 of "Quasar-KVO" complex [1]. The BRAS allows to register wideband signals of 512 MHz, that provides the necessary sensitivity for astrometrical observations. However, most existing VLBI radio telescopes still use data acquisition systems with narrowband channels (up to 16 MHz bandwidth). It greatly complicates the processing of joint observations of RT-13 with other VLBI radio telescopes.

To achieve a compatibility of RT-13 with radio telescopes, equipped with narrow-band backend, BRAS will be supplement with an external digital downconverter bank (DDCB). The paper presents principles, features and implementation details of DDCB.

2 System structure

DDCB includes three optical receiver that provide the physical layer for transmitting and receiving the data flows through 10 Gbit/s Ethernet fiber-optic lines, digital signal conversion module that is implemented on the field

programmable logic gate array (FPGA), Ethernet interface controller and two local reference oscillators.

Three 10GE DBBC channels are required to simultaneously receive data of two X and one S freqency bands from the BRAS outputs. This provides a regular geodesic observation mode with frequency synthesis in 270 MHz at S and 720 MHz at X bands respectively.

Ethernet packets containing VDIF data [2], introduced in FPGA through GTX receiving ports using 10-gigabit SFP + transceivers. FPGA performs the next operations: buffering data, transformation specified spectrum areas to video frequency, formation an output data, containing 16 narrowband channels in VDIF format. Output data from FPGA GTX port through the optical transceiver SFP + are transmitted to the data buffer device by 10GE Interface.

DDCB is controlled by a radio telescope central computer via 10/100/1000 Ethernet interfaces. Microblaze processor for control is implemented in the FPGA configuration.

3 The digital signal conversion module

Digital converter module is implemented on FPGA XC7325T-2FFFG900 and contains three independent data buffers, the three prefilters, 16-channel switch and 16 digital frequency converters. The processing of digital flows in each downconverter is divided into several stages: separation of the upper and lower sideband signal after prefiltration stage, moving a predetermined portion of the spectrum to lower frequencies, video bandwidth forming and subsequent formation of two-bit data flow. In addition, the FPGA configuration contain timer, VDIF frame data pack unit, Ethernet frame pack unit, data-capture module and Microblaze control processor.

Each data buffer unit parses packet headers and extracts the data sequences, then restores continuous digital data stream with rate of up to 8 Gb/s (eight eight-bit samples with a clock frequency of 128 MHz). Prefiltration is produced by polyphase filter that was constructed on the discrete Fourier transform basis with pre-formed an amplitude-frequency characteristic by using a weighting function [3].

The order for shaping filters is chosen equal to 8. The initial bandwidth of 512 MHz is divided into $M = 8$ overlapping ranges of 128 MHz. The advantage of this signal pre-filtering with the partition is the save FPGA resources and the relative ease of implementation. Disadvantages of this method include the fact that $i\cdot$ 128 MHz ($i = 0 \dots M - 1$) frequency of signal is transformed to the zero frequency ("blind zone"), as well as necessary to deal with a quadrature signal. The transform of any signal portion in the band $0 - 512$ MHz, including those frequencies around $128 \cdot i$ MHz $\pm\Delta f$, where Δf — bandwidth video filter output (in this case, 8 or 16 MHz) is provided

through a complementary additional quadrature converter to 32 MHz, which provide the possibility to processing of “blind spots”.

Through switch quadrature signals from polyphase filter bank are fed to the sidebands separator. Separation sideband is performed by phase method. To effectively use the resources of the FPGA low-frequency spectrum of the signal is advantageous to process separate from the main part of the spectrum, simplifying the process and the last [4].

To troubleshoot “bundled” sine filter frequency response at higher frequencies close to the Nyquist frequency, in the structure included two spectrum inverters — one inlet and one outlet. The total bandwidth of the filter separator is chosen equal from 0.15 to 52 MHz, and if necessary, the spectrum processing section, starting from 52 MHz up to the Nyquist frequency with spectrum inversion mode by “switch on” inverters at the inlet and outlet. The achieved suppressing coefficient of side bands in most of the working strip of separator is no less than 35 dB.

The next step of processing is performed by digital transformation of the signal. The frequency converter comprises quadrature mixer, quadrature frequency oscillator that operating in a range of 0—63.99 MHz, filter-decimator with a decimation factor of 2 times and sidebands separator, operating from 0.1 to 25 MHz. Sidebands separator is built on the principles described above, but additionally uses a partition of the entire frequency band signal into 3 sub-band. The output of the frequency converter is switchable filter 8/16 MHz. Step of quadrature tuning oscillator, that constructed on the basis of the sine and cosine tables, is 10 kHz.

Two-bit quantizer with floating threshold is based on calculating the root mean square value of signal on a predetermined time interval and comparators.

The output formatter of VDIF-frame integrates the data from downconverter outputs into total flow, which is then broken up into packets of a given size. The frame headers include service information obtained by decoding the input data from BRAS, and additional parameters DDCB. These observations data together with service information packed in “raw” Ethernet-packets with the possible addition of UDP and IP headers, that transmitted through the interface to the transceiver 10GE receiver-transmitter and a next to the data buffering device on radio telescope.

4 The software

The controller was made on the basis of Microblaze-processor, which formed in FPGA, is the main element of DDCB management system. Upon request, obtained via Ethernet, the controller forms the response, which contains control information (e. g., synchronization check, presence of transcei-

vers and others). The obtained data are used to control system operation. To communicate with a computer through UDP FPGA use Ethernet-controller PHY 88E1111 and GMII interface. Text commands of UDP-packets from control computer are processed by Microblaze-processor which was formed in FPGA.

5 Conclusion

The main DDCB components were developed and debugged: data buffer, prefiltering, sidebands separator and digital down convertor, and output signal quantizer. The final adjustment of developed firmware is carrying out to optimize FPGA resource utilization. Laboratory tests of DDCB are currently performing and the first test in real observations has to be performed until the end of 2016.

References

1. *Nosov E., Berdnikov A., Grenkov S., etc.* Current Development State of the Russian VLBI Broadband Acquisition System. // IVS 2014 General Meeting Proceedings. Science Press, Beijing, China. — 2014. — P. 82–85.
2. *Whitney A., Kettenis M., Phillips C., etc.* VLBI Data Interchange Format (VDIF) // Proc. of the 8th International e-VLBI Workshop. Madrid. Spain. — 2009. — Vol. 51. — P. 42.
3. *Vaidyanathan P. P.* Mulitrate digital filter banks, polyphase networks, and applications: a tutorial // Proc. of IEEE. — 1990. — Vol. 78, N 1. — P. 56–93.
4. *Nosov E.* Digital baseband converter for data acquisition system of VLBI-radiotelescope // The IAA RAS journal. — 2010. — Vol. 21. — P. 99–105.