Extending Facility of BRAS by External Digital Downconverter Bank

Sergey Grenkov, Dmitry Marshalov, Evgeny Nosov

Institute of Applied Astronomy, Russian Academy of Sciences, St. Petersburg, 191187 Russia

1. Introduction

Broadband Acquisition System (BRAS) are used on fast slew radio telescopes RT-13 of complex "Quasar-KVO" with a diameter primary mirror 13.2 meters [1-5]. The BRAS allow to register signals in a relatively high frequency band (512 MHz), that provides the necessary sensitivity during astrometrical observations. However, most radio telescopes working for VLBI, still use conversion and registration system with narrowband channels (up to 16 MHz frequency band). This fact greatly complicates the conduct of joint observations on the RT-13 with other VLBI radio telescopes.

For compatibility of the RT-13 with other radio telescopes, equipped with narrow-band signal conditioning systems, it is proposed to supplement the BRAS with bank of external digital downconverter (BEDC). Principles, features and implementation of the BEDC are present in this poster.

2. The purpose and structure of the system

Most of the VLBI observations conducted in an international network using the method of frequency synthesis of S and X frequency bands [6]. In the low frequency range band arrangement of 6 narrowband channels does not exceed the bandwidth of BRAS channel and is about 270 MHz. For a standard arrangement of 8 narrowband channels in the X frequency band (720 MHz) is required two channels of BRAS. Thus, on entry BEDC must simultaneously receive the digital sequences from three BRAS channels and form output stream with the data from 14 independent narrowband channels. The input data format for BEDC is VDIF (VLBI Data Interchange Format [7]). The speed (2 or 8 Gbit/s) of the received input data stream for broadband channel are depends on the bits (2 or 8 bit) per samples in data flow. For compatibility with existing data buffering and transmission system [8] output format is VDIF. The output data stream contains selected portions of the spectrum width of 8 or 16 MHz (up to 14 parts) of any part of the three input broadband signal and does not exceed 4,096 Mbit / s (including the fact that the bit data output of 8 bits, and the number of channels supplemented by two "zero" tracks and total number of channels is 16 (in accordance with the requirements VDIF).

BEDC (Fig. 1) includes three optical transceiver that provide the physical layer for sending and receiving the data flows through the 10 Gbit / s Ethernet fiber-optic lines (FOL), the module for digital signal conversion by the field programmable logic gate array (FPGA), Ethernet interface controller and the oscillators of reference signals.

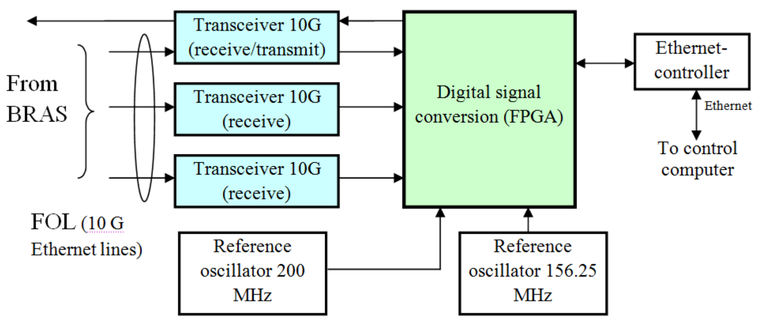

Fig. 1. Block diagram of the bank external digital downconverters for the BRAS.

Ethernet data packets, that contain VDIF data, via GTX receiving ports entered to the FPGA from a 10-gigabit transceivers, such as SFP +. In the FPGA is performed the next operations: buffering the data streams, transformation specified areas of spectrum to video frequency, forming an output and traffic information data in the format VDIF, that combining digital signals from 14 narrowband channels. Output data through the FPGA GTX transmitter port and an optical transceiver SFP + transferred to the data buffering device of the 10GE Interface.

BEDC controlled from a central computer of the radio telescope via 10/100/1000 Ethernet interfaces that implemented on a chip Marvell 88E1111 conjugated with FPGA. Microblaze processor for control is implemented in the FPGA configuration.

3. The digital signal conversion unit

Digital converter module is implemented on FPGA XC7325T-2FFFG900 and contains three independent channels for receiving and buffering of samples of the digital signal, the three pre-filter signals module, switch module and 14 channels for implementing digital downconverter function. The processing of digital flows in each downconverter is divided into several stages: separation of the upper and lower sideband signal after pre-filtration stage, carrying a predetermined portion of the spectrum to lower frequencies, video bandwidth forming and subsequent formation of two-bit data flow. In addition, the FPGA configuration are contain the timer module, VDIF frame data pack unit, Ethernet frame pack unit, data-capture module and Microblaze control processor (Fig. 2).

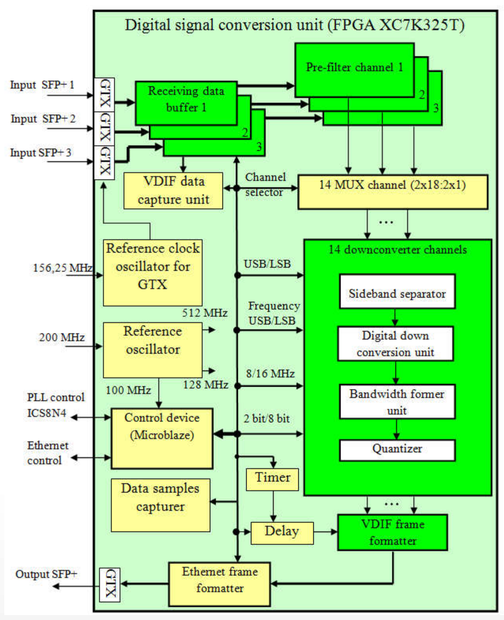

Fig. 2. Block diagram of digital conversion module

Each channel of data buffer unit receives 10G Ethernet perform packet parsing headers and extract samples of the signal sequence, which is then buffered in order to restore the continuous digital data stream at a rate of up to 8 Gb / s (eight eight-bit samples with a clock frequency of 128 MHz) to the pre-filtration.

Prefiltration produced by polyphasic filter that constructed on the basis of the discrete Fourier transform (DFT) with pre-formed an amplitude -frequency characteristic (AFC) by using a weighting function. The calculation of polyphase decomposition of signals is carried out according to the formula $y_k[n_k] = \sum_{i=0}^{M-1} h_k x[n_k] W_M^{-ki}$ [9]:

there M – the number of channels for polyphasic decomposition (the size of DFT), y_k – the samples of signal on the k-filters exit (k=0…M – 1), x – digital signal on the input of polyphasic filter; h – the weight function of analysis filter for pre-forming of filters frequency response, $W_M = e^{\frac{-j2\pi}{M}}$ – the complex Fourier transform's coefficient, n_k=integer(t/M)+k – the number of samples for channel k, t – the number of samples for filter input sequency, $j = \sqrt{1}$.

The choice coefficients of a weighting function substantially affects the channel impulse response and polyphase energy distribution between the main and side lobes of its spectral function. Therefore, to minimize the effects of spectral leakage in accordance with the recommendations in [10] the weighting function coefficients was calculated by the formula:

$$h[i] = \frac{1}{2} - \frac{1}{2}\cos\left(\frac{2\pi i}{pM}\right)\mathrm{sinc}\left(\frac{i - pM/2}{p}\right)$$

there p – order of the weighting function filter shaper in the channel of polyphase filter, i = 0...pM.

The order for shaping filters is chosen equal to 8. The initial bandwidth of 512 MHz is divided into M = 8 overlapping ranges of 128 MHz. The advantage of this signal prefiltering with the partition is the save FPGA resources and the relative ease of implementation. Disadvantages of this method include the fact that i 128 MHz (i = 0 ... M – 1) frequency of signal is transformed to the zero frequency ("blind zone"), as well as the need to work with a quadrature signal. The transform of any signal portion in the band 0 – 512 MHz, including those frequencies around 128 i MHz ± Δf, where Δf – bandwidth video filter output (in this case, 8 or 16 MHz) is provided through a complementary additional quadrature converter to 32MHz (Fig. 3), which provide the possibility to processing of "blind spots".

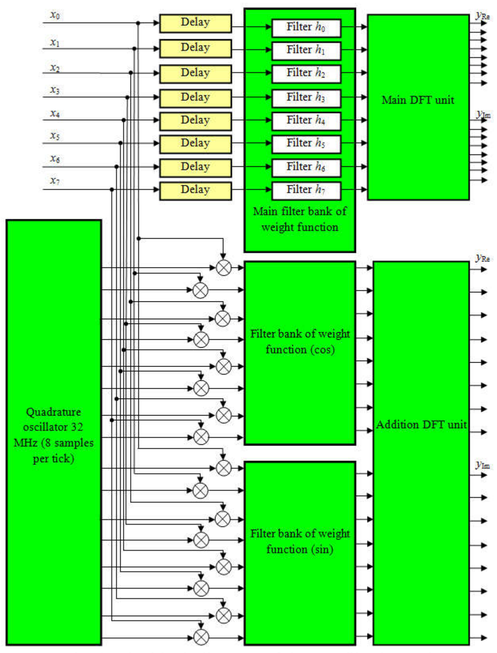

Fig. 3. The block diagram of the pre-filtering unit

The AFC of 5 major pre-filtered zones (solid lines) and 3 shifted by 32 MHz zones (dashed line) are shown in Fig. 4.

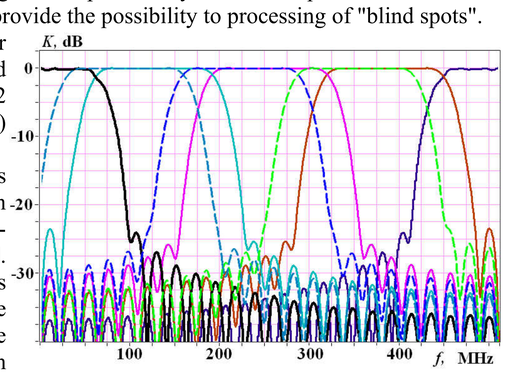

Fig. 4. The AFC of major pre-filtered zones (solid lines) and shifted by 32 MHz zones (dashed line)

Quadrature signals are fed via a switch on the upper and lower separator sideband signal. Separation sideband is performed by phase method. To ensure downconverter bottom border strip at least 1 MHz (in this frequency usually located the phase calibration signal), the broadband phase shift of one of the quadrature signals is needed [11]. According to the methods the quadrature signal passed throught the cosine and sine filters, that frequency responses build by the base proto-filters. The sine filter has phase shift 90° comparison to the cosine filter. In order to ensure the passage of the signal at a frequency of 1 MHz with a bandwidth of, for example, 32 MHz, requires the implementation of a narrow transition band frequency response (0.3% of the Nyquist frequency). The hardware implementation of narrow transition band with direct methods requires a large number of FPGA resources (the number of taps of the filter is inversely proportional to transition band), such as hardware multipliers, and in this case, due to the rather large number of channels is not applicable. To effectively use the resources of the FPGA low-frequency spectrum of the signal is advantageous to process separate from the main part of the spectrum, simplifying the process and the last [12]. It is also used for minimize the number of multipliers the method of multi-use FPGA resources with decreasing frequency (decimation) of the input signal. In accordance with the method that described in [12], the signal band with the prefilter output is divided into three sub-band (Fig. 5).

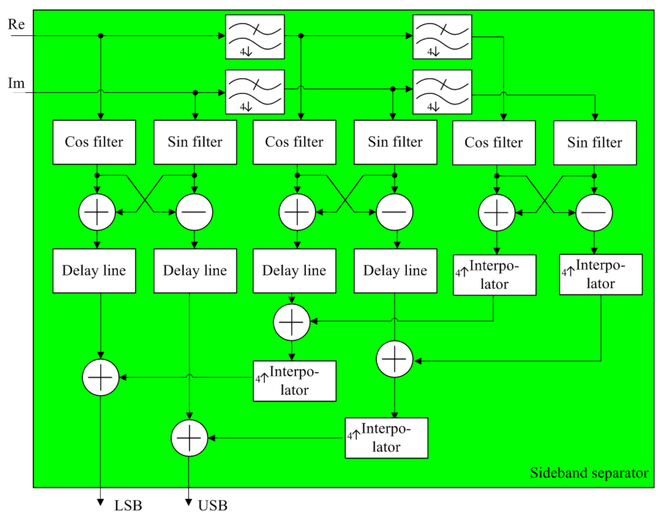

Fig. 5. The block diagram of separator for upper and lower sidebands (SSB).

To troubleshoot 'bundled' sine filter frequency response at higher frequencies close to the Nyquist frequency, in the structure included two spectrum inverters - one inlet and one outlet. The total bandwidth of the filter separator is chosen equal from 0.15 to 52 MHz, and if necessary, the spectrum processing section, starting from 52 MHz up to the Nyquist frequency with spectrum inversion mode by "switch on" inverters at the inlet and outlet. The frequency dependence of the separator and the frequency response are shown in Fig. 6. As can be seen from the graph of Fig. 6, the coefficient suppressing the side bands in most of the working strip of separator is no less than 35 dB.

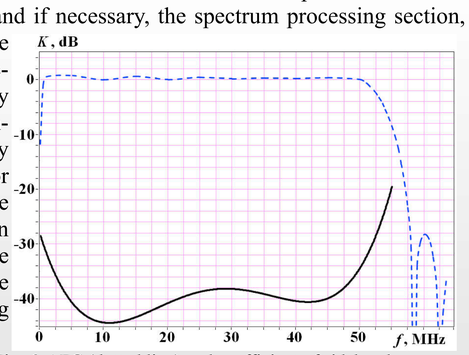

Fig. 6. AFC (dotted line) and coefficient of sideband suppression (solid line).

The next step of processing is performed by digital transformation of the signal. The frequency converter comprises (Fig. 7) quadrature mixer, quadrature frequency oscillator that operating in a range of 0 – 63.99 MHz, the filter-decimator with a decimation factor of 2 times and SSB, operating at frequencies from 0.1 to 25 MHz. SSB is built on the principles described above, also using a partition of the entire frequency band signal into 3 subband. The output of the frequency converter is switchable filter 8/16 MHz. Step of quadrature tuning oscillator, that constructed on the basis of the sine and cosine tables, is 10 kHz.

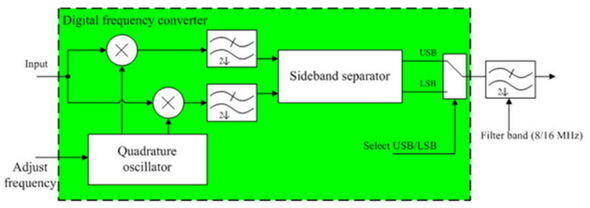

Fig. 7. The block diagram of frequency signal transformation unit

Two-bit quantizer with floating threshold is based on calculating the RMS value (RMS) signal σ_u on a predetermined time interval and comparators. The quantization of the amplitudes on the levels is performed in accordance with the following relationships: $u < -\sigma_u$, $-\sigma_u < u < 0$, $0 < u < \sigma_u$ и $u > \sigma_u$, there u – the instantaneous value of the voltage.

The output formatter of VDIF-frame integrates the data from downconverter outputs into total flow, which is then broken up into packets of a given size. The frame headers include service information obtained by decoding the input data from BRAS, and additional parameters BEDC. These observations together with service information packed in "raw» Ethernet-packets with the possible addition of UDP and IP headers, that transmitted through the interface to the transceiver 10GE receiver-transmitter and a next to the data buffering device on radio telescope.

4. The software

The controller was made on the basis of Microblaze-processor, that formed in FPGA, is the main element of BEDC management system. Upon request, obtained via Ethernet, the controller forms the response, that contains control information (eg, information about the presence of synchronization with the reference clock signal, the presence of transceivers on receive slots and decoding the data stream from the transceiver, and others). The data obtained are used to control system operation.

The system is controlled by a central computer of the radio telescope via the 10/100/1000 Ethernet interface. To communicate with a computer via UDP using Ethernet-controller PHY 88E1111, interfaced to the FPGA on the GMII interface. UDP-packets of control computer containing the text commands, entered to the formed in FPGA to Microblaze-processor, where they are processed.

All control and monitoring functions are implemented in the control program written in C ++ in a cross-platform environment for programming Qt 4.8. An example of the main tab of the graphical interface of the program on the computer screen is shown in Fig. 8.

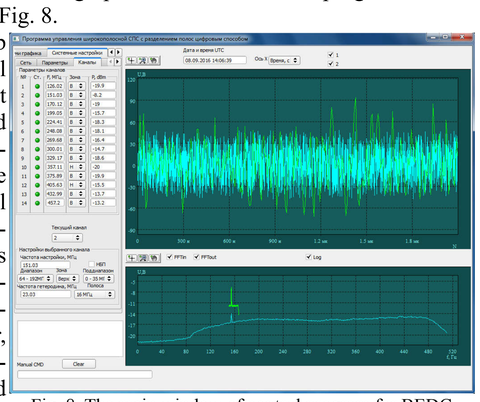

Fig. 8. The main window of control program for BEDC

On the main tab ("Channels") of the control program displays the current settings of each narrowband channel and power measurement data, display the "correctness" of the channel signals quantization statistics, as well as the settings panel of the parameter channel. On the "Settings" is displayed current DAS timer, the presence of synchronization with the time scale and time of commencement and completion of the "record". From this tab, you can set the time or select the reference data channel with which synchronization is performed. Set configuration and data transfer modes via 10G Ethernet can use with the "Recording Settings" tab. Tab "Inputs 10G» allows you to customize the behavior of foster 10G transceivers, as well as the control data received by the capture of data from VDIF-frame. Signal data are displayed as a waveform and spectrum, and service information from headers VDIF frames displayed in a tabular format.

5. Conclusion

Currently, the BEDC main components is developed and debugged: a buffer in receiving a data stream, the pre-filtering unit, the separator sidebands and spectral transform units and quantizer of the output signal. The project is at the final stage, the fine finishing processes are carrying out under blocks and parameters to optimize the configuration of FPGA with a view to the most efficient use of resources. Laboratory tests of BEDC layout planned for the end of September, and finish the test objects on observatories planned by the end of 2016.

REFERENCES

1. Ipatov A. A new generation of radio interferometers for basic and applied research // Successes of physical sciences. - M .: 2013. - T. 183, number 5. - P.769.
2. Ipatov A., Ivanov D., Ilin G., Olifirov V., Mardyshkin V., Surkis I., Fedotov L., Gayazov I., Stempkovsky V., Bondarenko Y. Russian Radio Interferometer of New Generation. // Proceedings of the 22nd European VLBI Group for Geodesy and Astrometry Working Meeting. 2015. – P. 75-79.
3. Grenkov S.A., Kol'tsov N.E., Nosov E.V., Fedotov L.V. The digital data acquisition system for astronomical radio interferometers with small antennas // Instruments and Experimental Techniques, 2011, № 6, c. 21–26.
4. Nosov E., Berdnikov A., Grenkov S., Marshalov D., Melnikov A., Fedotov L. Current Development State of the Russian VLBI Broadband Acquisition System. //IVS 2014 General Meeting Proceedings. Science Press, Beijing, China. P.82-85.
5. Melnikov A., Berdnikov A., Grenkov S., Marshalov D., Mikhailov A., Nosov E., Fedotov L. First Fringes with BRAS on VLBI Network "Quasar". //IVS 2014 General Meeting Proceedings. Science Press, Beijing, China. P.134-137.
6. Thompson, A. R.; Moran, J. M.Swenson, G. W. Interferometry and synthesis in radio astronomy. – M.:Fizmatlit, 2003. – 624 c.
7. Whitney A., Kettenis M., Phillips C., et al. VLBI Data Interchange Format (VDIF) // Proc. of the 8th International e-VLBI Workshop. 22-26 June 2009. Madrid. Spain. P. 42.
8. Bezrukov I.A., Salnikov A.I., Yakovlev V.A., Vylegzhanin A.V. Russian Data Recoeding System of New Generation Система буферизации и передачи данных нового поколения. IAA RAS, 2015, vol. 32, pp. 3-9.
9. Vaidyanathan P.P., Mulitrate digital filter banks, polyphase networks, and applications: a tutorial, Proc. of IEEE, vol. 78 № I, Pages 56-93, 1990.
10. Christopher H. and Karen H. A Mathematical Review of Polyphase Filterbank Implementations for Radio Astronomy // Publications of the Astronomical Society of Australia, 2011, 28, PP. 317–322.
11. Lyons R. Understanding Digital Signal Processing.Pearson Education Inc, 2004.
12. Nosov E.V. Digital baseband converter for data acquisition system of VLBI-radiotelescope // IAA RAS, vol. 21, 2010, pp. 99-105.